What is claimed is:

1. A method for manufacturing a semiconductor device, comprising the steps of:

providing a semiconductor substrate;

forming an interlayer insulating layer on the semiconductor substrate;

forming a contact hole in the interlayer insulating layer;

forming a plug recessed inside the contact hole;

forming an ohmic contact layer on the plug;

depositing a layer selected from the group consisting of an La layer and a LaN layer on the ohmic contact layer;

performing a nitridation process by a plasma treatment process to form a LaN diffusion barrier layer on the ohmic contact layer; and

sequentially forming a bottom electrode, a BLT ($(Bi_xLa_y)Ti_3O_{12}$) dielectric layer and a top electrode on the entire structure.

2. The method as recited in claim 1, wherein the LaN diffusion barrier layer is formed at thickness of 500 Å to 2000 Å.

3. The method as recited in claim 2, wherein the step of depositing the La or LaN layer is performed by a deposition technique selected from the group consisting of pulse laser

deposition (PLD), physical vapor deposition (PVD), metal organic chemical vapor deposition (MOCVD), sputtering, plasma enhanced metal organic chemical vapor deposition (PEMOCVD), liquid source mist chemical deposition (LSMCD) and atomic layer deposition (ALD).

4. The method as recited in claim 1, wherein in the step of performing a nitridation process, the plasma treatment process is performed at a pressure of 1 mtorr to 10 torr, at a power of 25 W to 500 W and at a wafer temperature of 250 ℃ to 650 ℃.

5. The method as recited in claim 1, wherein, in the step of sequentially forming a bottom electrode, a BLT dielectric layer and a top electrode, the atomic concentration of Bi in the BLT dielectric layer is 3.25 to 3.35 and the atomic concentration of La is 0.80 to 0.90.

6. The method as recited in claim 1, wherein in the step of sequentially forming a bottom electrode, a BLT dielectric layer and a top electrode, the bottom electrode and the BLT dielectric layer are formed by a deposition technique selected from the group consisting of spin-on, physical vapor deposition, metal organics chemical vapor deposition, metal organic deposition, plasma enhanced chemical vapor deposition, liquid source mist chemical deposition and atomic

layer deposition.

7. The method as recited in claim 6, wherein the plasma enhanced chemical vapor deposition is performed at a pressure of 5 mtorr to 50 torr and at a temperature of 400 ℃ to 700 ℃.

8. The method as recited in claim 6, wherein the MOD technique is carried out by steps including performing a first thermal treatment process for nucleation of the BLT layer and performing a second thermal treatment process for crystallization of the BLT layer.

9. The method as recited in claim 8, wherein the first thermal treatment process is performed by a rapid thermal process (RTP) at a speed of 80 ℃/second to 300 ℃/second and in an ambient of a reaction gas selected from the group consisting of an oxygen gas, a N_2O gas and a mixture gas of an oxygen gas and a N_2O gas.

10. The method as recited in claim 8, wherein the second thermal treatment process is performed at a temperature of 650 ℃ to 675 ℃ in an ambient selected from the group consisting of an oxygen gas, a N_2O gas and a mixture gas of oxygen gas and N_2O.

11. The method as recited in claim 1, wherein in the step of sequentially forming a bottom electrode, a BLT dielectric layer and a top electrode, the top electrode is formed of a material selected from the group consisting of IrO_2, Ru, Pt and RuO_x, wherein x is an integer from 1 to 3.

12. The method as recited in claim 1, wherein in the step of sequentially forming a bottom electrode, a BLT dielectric layer and a top electrode, the top electrode is formed by a deposition technique selected from the group consisting of metal organic chemical vapor deposition (MOCVD), physical vapor deposition (PVD), spin-on and plasma enhanced metal organic chemical vapor deposition (PEMOCVD).

13. The method as recited in claim 1, wherein in the step of sequentially forming a bottom electrode, a BLT dielectric layer and a top electrode, the bottom electrode is formed as a type selected from the group consisting of a flat type, a cylinder type and a concave type.

14. A semiconductor device, comprising:

a semiconductor substrate;

a transistor including a gate insulating layer and a gate electrode formed on the semiconductor substrate and a source/drain region formed in the semiconductor substrate;

a contact hole exposing the source/drain region;

a plug recessed inside the contact hole;

an ohmic contact layer formed on the plug;

an LaN diffusion barrier layer formed on the ohmic contact layer;

a bottom electrode on the LaN diffusion barrier layer;

a dielectric layer formed by a BLT ($(Bi_xLa_y)Ti_3O_{12}$) layer on the bottom electrode; and

a top electrode formed on the dielectric layer.

15. The semiconductor device as recited in claim 14, wherein, in the BLT layer, the atomic concentration of Bi is 3.25 to 3.35 and the atomic concentration of La is 0.80 to 0.90.

16. The semiconductor device as recited in claim 14, wherein the top electrode is formed of a material selected from the group consisting of IrO_2, Ru, Pt and RuO_x, wherein x is an integer 1 to 3.

17. The semiconductor device as recited in claim 14, wherein the bottom electrode is formed as a type selected from the group consisting of a flat type, a cylinder type and a concave type.